

Docket: XA-9472

Supplemental Application Data Sheet**Application Information**

Application Number::	09/855,660
Filing Date::	05/16/2001
Application Type::	Regular
Subject Matter::	Utility
Suggested Classification::	326-121
Suggested Group Art Unit::	2819
CD-ROM or CD-R?	None
Title::	SEMICONDUCTOR INTEGRATED CIRCUIT HAVING HIGH-SPEED AND LOW-POWER LOGIC GATES WITH COMMON TRANSISTOR SUBSTRATE POTENTIALS, AND DESIGN DATA RECORDING MEDIUM THEREFOR
Attorney Docket Number::	XA-9472
Request for Early Publication?::	No
Request for Non-Publication?::	No
Suggested Drawing Figure::	1
Total Drawing Sheets::	22
Small Entity::	No
Petition included?::	No
Secrecy Order in Parent Appl.?::	No

Applicant Information

Applicant Authority type::	Inventor
Primary Citizenship Country::	Japan
Status::	Full Capacity
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Middle Name::	
Family Name::	Shimazaki

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Applicant Authority type:: Inventor
Primary Citizenship Country:: Japan
Status:: Full Capacity
Given Name:: Motoi
Middle Name::
Family Name:: Ichihashi
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Correspondence Information

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Representative Information

Representative Customer Number::	181

Representative Designation::	Registration number::	Name::
Primary	31,568	Mitchell W. Shapiro

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application			

Foreign Priority Information

Country::	Application Number::	Filing Date::	Priority Claimed::
Japan	2000-152732	05/19/2000	Yes

Assignee Information

Assignee Name:: **Renesas Technology, Corp.**
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Country of mailing address:: Japan

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